REMARKS

In the non-final Office Action, the Examiner objects to claim 1 based upon informalities; rejects claims 1, 2, 7, 8, 14 and 15 under 35 USC §103(a) as being unpatentable over Chen et al. (US Patent No. 6,005,377) in view of Asato et al. (US Patent No. 5,212,782); objects to claims 3-6, 9-13 and 16-19 as being dependent upon a rejected base claim but allowable if rewritten in independent form including all of the features of the base claim and any intervening claims; and allows claims 20-24 and 26-31.

By way of the present amendment, Applicant amends claims 1, 11, 13, 14 and 26 to improve form. No new matter has been added by way of the present amendment. Claims 1-31 remain pending in the instant application.

Applicant notes with appreciation the indication that claims 20-24 and 26-31 are allowable over the art of record and that claims 3-6, 9-13 and 16-19 would be allowable if rewritten into independent form to include all the features of the base claim and any intervening claims. Applicant respectfully points out that claim 25 depends from allowed claim 20. Claim 25 is not discussed on page 4 of the Office Action in conjunction with the other allowed claims. Applicant believes that claim 25 is allowable and respectfully requests that claim 25 be identified as allowable in subsequent correspondence from the Examiner.

Claim Objections

The Examiner objects to claim 1 because the phrase "dynamically selectively delay" on line 10 should read as "dynamically and selectively delay" (Office Action, page 2). Applicant has amended claim 1 so the phrase now reads as "dynamically and selectively delay." Applicant respectfully requests reconsideration and withdrawal of the objection to clam 1.

35 USC §103 Rejections

Claims 1, 2, 7, 8, 14 and 15 stand rejected under 35 USC §103(a) as being unpatentable over Chen in view of Asato. Applicant respectfully traverses this rejection.

A proper rejection under 35 USC §103 requires that three basic criteria are met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim features. Furthermore, the teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, not in applicant's disclosure (M.P.E.P. 2143.03). Chen and Asato, alone or in combination, do not teach or suggest the features of claims 1, 2, 7, 8, 14 and 15.

Independent claim 1 is directed to a method for designing digital signal processing hardware to implement a z-domain transfer function, wherein the processing of signal samples is characterized by constant latency. The method includes specifying the transfer function; without regard to latency characteristics, specifying a first hardware stage to process the signal samples in accordance with the transfer function; and, specifying a second hardware stage to dynamically and selectively delay the signal samples processed by the first hardware stage such that the combined first and second stage latency for the processing of the signal samples is a constant. Chen and Asato, whether taken alone or in any reasonable combination, do not disclose or suggest the combination of features of claim 1.

For example, Chen and Asato do not disclose or suggest specifying, without regard to

latency characteristics, a first hardware stage to process the signal samples in accordance with the transfer function. The Examiner relies on Chen, Figure 3 and col. 6, lines 51-65, for allegedly disclosing this feature (Office Action, page 3). Applicant disagrees.

At col. 6, lines 51-65, Chen discloses:

> FIG. 3 is a simplified block diagram of a example PWM generator 128 according to the general principles of the present invention. The generator 128 generally includes a data register 302, an up-down counter 304, a flip-flop 306, and a clock 308. When the digital value of the duty cycle is fed into the PWM generator 128 via line 127 it is captured in the data register 302. The value is then fed to the counter 304 via line 303, and used as a terminating point for counter 304. Accordingly, an up-counter termination signal is sent to the flip-flop 306, resulting in a signal (not shown) whose on-time is equal in length to the value initially stored in the date register 302, which is the desired duty cycle. Thus, at the end of the cycle, the counter 304 is reset and the flip-flop 306 will go inactive (or changes state) until the end of the entire cycle period, N bits.

This section of Chen discloses a PWM generator that receives a digital value associated with a duty cycle of a converter. This section of Chen does not disclose or suggest specifying, without regard to latency characteristics, a first hardware stage to process the signal samples in accordance with the transfer function, as required by claim 1.

Chen and Asato do not further disclose specifying a second hardware stage to dynamically and selectively delay the signal samples processed by the first hardware stage such that the combined first and second stage latency for the processing of the signal samples is a constant, as required by claim 1. The Examiner admits that Chen does not disclose this feature and relies on Figures 4, 6, and 7 and col. 2, lines 1-16, of Asato for allegedly disclosing this feature (Office Action, page 3). These sections of Asato do not disclose or suggest the above feature of claim 1.

Figure 4 of Asato depicts a carry-save array multiplier having piplining stages inserted between its adder stages to provide a higher output frequency since the multiplier is able to begin processing a second pair of numbers before completing processing on a first pair of numbers (col. 5, lines 28-35). Figure 4 in no way discloses or suggests specifying a second hardware stage to dynamically and selectively delay the signal samples processed by the first hardware stage such that the combined first and second stage latency for the processing of the signal samples is a constant, as required by claim 1. Therefore, Figure 4 of Asato does not cure the defects of Chen with respect to the above feature of claim 1.

Figure 6 of Asato depicts a multi-stage datapath element containing the multiplier of Figure 5 (Asato) with pipelining stages inserted such that there is a pipelining stage after every third carry-save adder. Figure 5, as referenced above, depicts an implementation of an N x M bit array multiplier consisting of an input buffer, carry-save adders and a ripple-carry adder (col. 6, lines 56-62). These figures of Asato in no way disclose or suggest specifying a second hardware stage to dynamically and selectively delay the signal samples processed by the first hardware stage such that the combined first and second stage latency for the processing of the signal samples is a constant, as required by claim 1. Therefore, Figures 5 and 6 of Asato do not cure the defects of Chen with respect to the above feature of claim 1.

Figure 7 of Asato depicts a generalized technique for inserting pipelining stages in multi-stage datapath elements (col. 7, lines 32-34). Figure 7 in no way discloses or suggests specifying a second hardware stage to dynamically and selectively delay the signal samples processed by the first hardware stage such that the combined first and second stage latency for the processing of the signal samples is a constant, as required by claim 1. Therefore, Figure 7 of Asato does not

cure the defects of Chen with respect to the above feature of claim 1.

At col. 2, lines 1-16, Asato discloses:

> Briefly, the present invention relates to a method for determining delays through multiple stage datapath elements. According to the present invention, the delay through each stage of the datapath element can be estimated in accordance with an equation such as:
> $D_s = D_b N_b + C$
> where D_s is the estimated stage delay, D_b is a delay associated with communication between bits in one stage, N_b is the number of bits in the datapath element, and C is a constant. Based upon the estimated delays, positions of pipelining stages in the datapath functional element can be calculated.

This section of Asato describes a method for determining delays through multiple stage datapath elements. Contrary to the Examiner's interpretation, this section of Asato does not disclose or suggest a second hardware stage to dynamically and selectively delay signal samples processed by the first hardware stage such that the combined first and second stage latency for the processing of the signal samples is a constant, as required by claim 1. If this 35 USC §103(a) rejection is maintained, Applicant respectfully requests that the Examiner explain how this section of Asato corresponds to the above feature of claim 1.

For at least the reasons above, Chen and Asato, taken alone or in any reasonable combination, fail to disclose or suggest the features of claim 1. Applicant respectfully requests that the rejection of claim 1 under 35 USC §103(a) based on the combination of Chen and Asato be reconsidered and withdrawn.

Claims 2, 7 and 8 depend from independent claim 1. Therefore, these claims are patentable over Chen and Asato, whether taken alone or in any reasonable combination, for at least the reasons given above with respect to claim 1. Moreover, these claims recite additional

features not disclosed or suggested by Chen and Asato. For example, claim 2 recites that the first hardware stage is a generic data processor. The Examiner alleges that Chen discloses this feature and points to col. 1, lines 50-56 in support of the allegation (Office Action, page 4). Applicant disagrees.

At col. 1, lines 50-56, Chen discloses:

> Despite the numerous limitations of analog circuitry, however, it remains the choice for use in a majority of commercially manufactured switch-mode converters today, because there are no suitable technology design alternatives available for switched-mode converters. Digital controllers have been successfully employed in place of analog controllers in slower power system designs such as Uninterruptible Power Supplies (UPSs)

This section of Chen discloses that digital controllers have been used in slower power system designs, such as UPSs. Contrary to the Examiner's allegation, this section of Chen does not disclose a first hardware stage that is a generic data processor, as required by claim 2. Applicant respectfully requests that the Examiner explain how this section of Chen teaches that a first hardware stage is a generic data processor, as required by claim 2, or withdraw the rejection.

For at least these additional reasons, Chen and Asato, taken alone or in any reasonable combination, fail to disclose or suggest the feature of claim 2. Applicant respectfully requests that the rejection of claim 2 under 35 USC §103(a) based on the combination of Chen and Asato be reconsidered and withdrawn.

Claim 7 recites specifying the target implementation technology independent of specifying the first hardware stage. With respect to the above feature of claim 7, the Examiner

alleges that Chen discloses a target technology, which is an FPGA and relies on col. 2, lines 49-56 in support of the allegation (Office Action, page 4). Applicant disagrees.

At col. 2, lines 49-56, Chen discloses:

> In an exemplary embodiment, the controller is a Field Programmable Gate Array (FPGA) with the ability to handle numerous functions simultaneously and in parallel, as opposed to a DSP which handles instructions serially. Thus, the controllers of the present invention can handle bandwidths greater than or equivalent to analog controllers, in the range of 5 kHz-to-100 kHz.

This section of Chen discloses a controller that is an FPGA. Contrary to the Examiner's allegation, this section of Chen does not teach specifying a target implementation technology independently of the first hardware stage, as required by claim 7. Applicant respectfully requests that the Examiner explain how this section of Chen teaches the feature of claim 7 or withdraw the rejection.

For at least these additional reasons, Chen and Asato, taken alone or in any reasonable combination, fail to disclose or suggest the feature of claim 7. Applicant respectfully requests that the rejection of claim 7 under 35 USC §103(a) based on the combination of Chen and Asato be reconsidered and withdrawn.

Claim 8 depends from claim 7 and recites that the target implementation technology is a design approach selected from the group consisting of FPGA, ASIC, semi-custom, and custom. The Examiner relies on col. 2, lines 49-56 of Chen for allegedly disclosing this feature (Office Action, page 4). Applicant disagrees.

At col. 2, lines 49-56, Chen discloses:

> In an exemplary embodiment, the controller is a Field Programmable Gate Array (FPGA) with the ability to handle numerous functions simultaneously and in parallel, as opposed to a DSP which handles instructions serially. Thus, the controllers of the present invention can handle bandwidths greater than or equivalent to analog controllers, in the range of 5 kHz-to-100 kHz.

This section of Chen discloses a controller that is an FPGA; however, this section of Chen does not disclose or suggest a target implementation technology that is a design approach selected from a group containing members consisting of ASIC, semi-custom and custom. Contrary to the Examiner's allegation, this section of Chen does not teach the feature of claim 8.

For at least these additional reasons, Chen and Asato, taken alone or in any reasonable combination, fail to disclose or suggest the feature of claim 8. Applicant respectfully requests that the rejection of claim 8 under 35 USC §103(a) based on the combination of Chen and Asato be reconsidered and withdrawn.

Claim 14 recites features similar to claim 1 and is believed allowable for reasons similar to reasons argued with respect to claim 1 above. Claim 15 depends from claim 14. Therefore, this claim is patentable over Chen and Asato for at least the reasons given above with respect to claim 14. Moreover, claim 15 recites features similar to claim 2 and is believed allowable for at least the reasons argued with respect to claim 2 above.

Conclusion

In view of the foregoing amendment and remarks, Applicant respectfully requests the Examiner's reconsideration of this application, and the timely allowance of the pending claims.

To the extent necessary, a petition for an extension of time under 37 C.F.R. § 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account No. 50-1070 and please credit any excess fees to such deposit account.

Respectfully submitted,

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